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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/682,863	10/25/2001	Donald Thomas McGrath	RD-27645	9978

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EXAMINER
SHINGLETON, MICHAEL B

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 05/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09-682,863	McGrath
Examiner	**Group Art Unit**
MICHAEL B SHINGLETON	2817

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 2-12-2002.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-24 is/are pending in the application.

Of the above claim(s) 6-9 is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-5 and 10-24 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☒ The drawing(s) filed on 12-3-2001 is/are not objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received: _____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☒ Notice of References Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

DETAILED ACTION

Applicant's election with traverse of the restriction requirement in Paper No. 4 is acknowledged. The traversal is on the ground(s) that Applicant believes that a thorough search and examination of either group would be relevant tot he examination of the other group and that requirements for restriction are not mandatory. This is not found persuasive because The search for the buffered logic level shifting circuit is not required for the amplifier system. Furthermore, a significant additional burden would be placed on the examiner to examine and possibly reject the non-elected invention. Even if a restriction requirement is not mandatory, this does not mean that a restriction requirement cannot be made.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCartney 6,380,801 (McCartney) in view of Fujii et al. 5,184,199 (Fujii).

Figures 1 and 5 of McCartney disclose the basic arrangement and method of an operational amplifier employing choppers. A first chopper 102 (16) is placed after an input signal generator and before the input of a first amplifier and a second chopper 26 is placed between the output of the first amplifier and the input of the second amplifier. The amplifiers employ nmos transistors. McCartney fails to disclose the use of silicon carbide nmos depletion mode transistors, however, Fujii clearly points out that such nmos transistors operate under severe conditions like high temperature, high frequency, and radiation exposure and are "expected to have wide applications for devices" (See col. 1, lines 11-26). They are just better transistors compared to pure silicon based transistors.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the nmos transistors of McCartney with silicon carbide

nmos depletion transistors so as to enable operation under severe conditions as taught by Fujii.

McCartney also does not disclose the switching elements inside the choppers and the use of silicon carbide nmos depletion transistors for the choppers. Given the advantages of silicon carbide nmos depletion mode transistors as noted above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ such transistors for the chopper so as to take advantage of the operation under severe conditions as taught by Fujii. Note that a device is only as weak as its weakest link and thus it is only common sense to employ better transistors through out a circuit when one wants to operate it in severe conditions.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCarthey and Fujii as applied to claims 1-3 above, and further in view of Richter et al. 4647845 (Richter).

McCartney does not show the details of the device that makes the control signals for the chopper or the use of two nmos silicon carbide depletion transistors for the chopper, however, it is common place to employ as part of the conventional chopper and chopper control circuit two transistors for the chopper and a level shifter in the chopper control circuit so as to ensure that the two switches that must make up a chopper when the signal is applied to two nodes are not on at the same time. Such is shown in Figure 6 and described in column 4 around line 36 of Richter.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the conventional chopper control circuit like that of Richter in McCartney so as to control the two switches in the chopper of McCartney so as to ensure that the two switches are not turned on at the same time as taught by Richter.

Claims 10 and 14-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCartney 6,380,801 (McCartney) in view of Fujii et al. 5,184,199 (Fujii) and Richter et al. 4647845 (Richter).

Figures 1 and 5 of McCartney disclose the basic arrangement and method of an operational amplifier employing choppers. A first chopper 102 (16) is placed after an input signal generator and before the input of a first amplifier and a second chopper 26 is placed between the output of the first amplifier and the input of the second amplifier. The amplifiers employ nmos transistors. McCartney fails to disclose the use of silicon carbide nmos depletion mode transistors, however, Fujii clearly points out that such nmos transistors operate under severe conditions like high temperature, high frequency, and radiation exposure and are "expected to have wide applications for devices" (See col. 1, lines 11-26). They are just better transistors compared to pure silicon based transistors.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the nmos transistors of McCartney with silicon carbide nmos depletion transistors so as to enable operation under severe conditions as taught by Fujii.

McCartney also does not disclose the switching elements inside the choppers and the use of silicon carbide nmos depletion transistors for the choppers. Given the advantages of silicon carbide nmos depletion mode transistors as noted above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ such transistors for the chopper so as to take advantage of the operation under severe conditions as taught by Fujii. Note that a device is only as weak as its weakest link and thus it is only common sense to employ better transistors through out a circuit when one wants to operate it in severe conditions.

McCartney does not show the details of the device that makes the control signals for the chopper or the use of two nmos silicon carbide depletion transistors for the chopper, however, it is common place to employ as part of the conventional chopper and chopper control circuit two transistors for the chopper and a level shifter in the chopper control circuit so as to ensure that the two switches that must make up a

chopper when the signal is applied to two nodes are not on at the same time. Such is shown in Figure 6 and described in column 4 around line 36 of Richter.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the conventional chopper control circuit like that of Richter in McCartney so as to control the two switches in the chopper of McCartney so as to ensure that the two switches are not turned on at the same time as taught by Richter.

Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCartney 6,380,801 (McCartney) in view of Fujii et al. 5,184,199 (Fujii) and Richter et al. 4647845 (Richter) as applied to claims 10 and 14-24 above, and further in view of White et al. 4,558,235 (White)

The combination based on McCartney lacks the use of diodes in the level shifter.

Figure 1 White clearly shows the use of diode in the level shifter that forms a load impedance so that the level can be shifted. FETS connected to form a diode are well known art recognized equivalents to that of White.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize FET based diodes in the level shifter so as to from an impedance that enable the level shifting as taught White.

As to the use of resistor loads such are conventional art recognized equivalent loads in a level shifter and as such it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize resistors for the loads in the above McCartney, Fujii, Richter and White combination.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is 703-308-4903. The examiner can normally be reached on Mon-Thurs from 8:30 to 4:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (703) 308-4909. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MBS
May 1, 2002

MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817